Flexible Index Mapping Scheme for Packet-Level Index Modulation

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***Abstract*—Long range wide area network (LoRaWAN) attracts attention due to its ability to realize massive machine-type communication (MTC); however, the throughput is low due to its narrow-band transmission and chirp spread spectrum. Packet-level index modulation (PLIM) increases the throughput by utilizing a data packet's frequency channel and transmission timing as an information-bearing index. This letter proposes a flexible index mapping scheme to fully utilize the available frequency channels and transmission timings to increase the number of bits transmitted by an index and avoid packet collision. Numerical results show that the proposed scheme improves the throughput and significantly reduces the required memory size of end nodes.**

***Index Terms*—LPWAN, LoRaWAN, index modulation.**

I. Introduction

In RECENT years, with the development of the Internet-of-Things (IoT), low power wide area networks (LPWANs) that enable massive machine-type communication (MTC) have been attracting attention [1]–[3]. Packet collision due to simultaneous packet transmission from multiple end nodes (ENs) and a duty cycle (DC) that defines the over-the-air (OTA) ratio of each EN and GW [4] are the main factors to limit the throughput improvement of LPWAN. Long range wide area network (LoRaWAN) [5], which is a type of LPWAN, adopts chirp spread spectrum (CSS) modulation as the physical (PHY) layer technology to achieve long-range and low-power communication. Since LoRaWAN operates in unlicensed bands, other systems may interfere with the communication. Thus, it is necessary to avoid using specific frequency channels to avoid the interference. There are many works to avoid packet collision avoidance in LoRaWAN [6].

Packet-level index modulation (PLIM), which is a type of index modulation (IM) [7], is proposed in [8]. PLIM utilizes a frequency channel and transmission timing of a data packet as an information-bearing index to increase the throughput without changing the LoRaWAN standard under the constraint of DC. Computer simulation results demonstrate that PLIM can increase the throughput by up to 32.5% compared to the conventional LoRaWAN. However, three major issues must be solved to maximize the benefit of index transmission, i) periodic packet collision, ii) insufficient utilization of resources, and iii) overhead and memory size required for sharing and storing the mapping information. This letter proposes a flexible index mapping scheme for PLIM to overcome the three issues above. The proposed scheme maps an information bit sequence to an index to avoid packet collisions by maximizing the use of available frequency channels and time slots even when some frequency channels are not available. The proposed index mapping improves throughput by increasing the number of transmitted bits and reducing the packet collision rate. Moreover, the proposed index mapping does not require any information exchange between the EN and the GW, and it can significantly reduce the overhead and memory size.

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II. Packet-Level Index Modulation (PLIM)

A. Overview

Without loss of generality, we consider the communication between one specific EN and the GW over K frequency channels. This letter assumes that each EN generates data packets such as sensing information every $T_{\rm frame}$ [sec]. Frame length $T_{\rm frame}$ is split into Q non-overlapping time slots with equal time length $T_{\rm slot}$ [sec]. Once an information bit sequence $\mathbf{B} \in \{0,1\}^{B\times 1}$ of length B [bits] is generated, the EN divides $\mathbf{B}$ into payload bit sequence $\mathbf{B}_{\rm pl} \in \{0,1\}^{B_{\rm pl}\times 1}$ and PLIM bit sequence $\mathbf{B}_{\rm plim} \in \{0,1\}^{B_{\rm plim}\times 1}$. Here, $B_{\rm pl}$ and $B_{\rm plim}$ are the payload bit sequence length and the PLIM bit sequence length, respectively, i.e., $B_{\rm pl}+B_{\rm plim}=B$. The EN generates a data packet using $\mathbf{B}_{\rm pl}$ in the same way as the conventional LoRaWAN. The EN transmits the generated data packet at frequency channel $k \in \mathcal{K}=\{0,1,\ldots,K-1\}$ and time slot $q \in \mathcal{Q}=\{0,1,\ldots,Q-1\}$, which are determined by

$$(k,q)=\mathcal{F}(\mathbf{B}_{\rm plim}), \tag{1}$$

where $\mathcal{F}$ denotes an arbitrary index mapper.

Once the GW receives a packet on frequency channel $\tilde{k} \in \mathcal{K}$, the GW estimates time slot $\tilde{q} \in \mathcal{Q}$ [8]. The estimated frequency channel and time slots, $(\tilde{k},\tilde{q})$, are input to index demapper $\mathcal{F}^{-1}$, which demodulates PLIM bit sequence $\tilde{\mathbf{B}}_{\rm plim} \in \{0,1\}^{B_{\rm plim}\times 1}$ as

$$\tilde{\mathbf{B}}_{\rm plim}=\mathcal{F}^{-1}(\tilde{k},\tilde{q}). \tag{2}$$

B. Issues Need To Be Solved

Conventional PLIM [8] has three major issues that must be solved to maximize the benefit of index transmission. First,

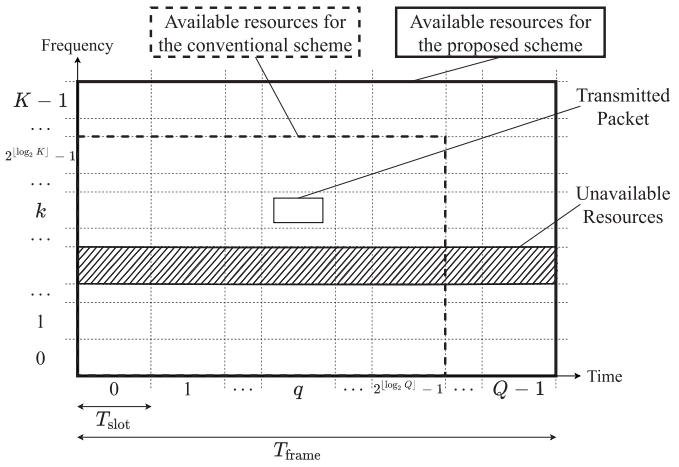

Fig. 1. Available resources for packet-level index modulation (PLIM).

periodic packet collisions may occur when some ENs select the same index. Second, PLIM has a constraint on the number of available resources. Since the conventional PLIM allocates PLIM bit sequence directly to frequency channels and time slots, it has the constraint that $\log_2 K, \log_2 Q \in \mathbb{N}^+$. Thus, the excessive resources of $(K \times Q - 2^{\lfloor \log_2 K \rfloor + \lfloor \log_2 Q \rfloor})$ cannot be used for index transmission as shown in Fig. 1. Third, a significant amount of overhead is required for index mapping updates. When the interference condition on a specific frequency channel changes by other systems using the same frequency channels, ENs and the GW exchange the index mapping. Thus, the network overhead or required memory at each EN becomes the system bottleneck.

To tackle the first issue, the authors in [9] have proposed a scheme to avoid periodic packet collisions. Specifically, PLIM bit sequence in decimal notation, D_{plim}, is shifted according to the EN's identification (ID) z and packet ID i as $D_{\text{plim}} = D'_{\text{plim}} + z \times i$, where D'_{plim} is the PLIM bit sequence in the first packet transmission and D_{plim} is cyclically shifted if $D_{\text{plim}} \geq 2^{\lfloor \log_2 K \rfloor + \lfloor \log_2 Q \rfloor}$. The bit-shifting is performed only when the same PLIM bit sequence is transmitted consecutively. When the PLIM bit-sequence changes, EN transmits a packet without bit-shifting. The same transmission resource may be used periodically even when the same information bit sequence is transmitted consecutively. An EN whose ID is approximately the number of resources always selects the same resource. For example, if $K = 4$, $Q = 4$, $z = 8$, and $D'_{\text{plim}} = 0$, then $D_{\text{plim}} = 0\ (2i \in \mathbb{N}^+), 8\ (2i - 1 \in \mathbb{N}^+)$, and the PLIM bit sequence of 0 and 8 is used periodically.

III. Proposed Scheme

This letter proposes a flexible index mapping scheme to fully utilize the available resources to increase the number of bits transmitted by an index and avoid packet collision. Specifically, we propose index mapper $\mathcal{F}$ and index de-mapper $\mathcal{F}^{-1}$ that utilize device address $\mathbf{B}_{\text{addr}}$ and packet counter $\mathbf{B}_{\text{pcnt}}$ contained in the header of LoRaWAN packets [5]. Index mapper $\mathcal{F}$ converts PLIM bit sequence $\mathbf{B}_{\text{plim}}$ into index of transmission frequency channel and time slot (k, q), and index de-mapper $\mathcal{F}^{-1}$ converts index of frequency channel and time slot of the received packet $(\tilde{k}, \tilde{q})$ into PLIM bit sequence $\tilde{\mathbf{B}}_{\text{plim}}$, respectively. The device address, $\mathbf{B}_{\text{addr}}$, is an EN-specific value expressed in 4 bytes, and packet counter $\mathbf{B}_{\text{pcnt}}$ is a packet-specific value expressed in 2 bytes, respectively. Thus, the proposed scheme solves several issues of [8] and [9]. Let us denote the available frequency channel set as $\mathcal{A} = \{a_0, a_1, \ldots, a_k, \ldots, a_{K-1}\}$, where $a_k \in \{0, 1\}$ is the state of frequency channel k. When frequency channel k is available, $a_k = 1$, otherwise $a_k = 0$. Number of available frequency channels K_{a} can be expressed as $K_{\text{a}} = \sum_{k=0}^{K-1} a_k\ (0 < K_{\text{a}} \leq K)$. The number of available resources R can be expressed as $R = K_{\text{a}} \times Q$.

Algorithm 1 Proposed Index Mapper $\mathcal{F}$

Require: $\mathcal{K}$, $\mathcal{Q}$, $\mathcal{A}$, f {Pre-shared between EN and GW}
Require: $\mathbf{B}_{\text{plim}}$ {Obtained from information divider [8]}
Require: $\mathbf{B}_{\text{addr}}, \mathbf{B}_{\text{pcnt}}$ {Obtained from LoRaWAN header [5]}
Ensure: (k, q)
1: Convert $\mathbf{B}_{\text{plim}}$ into a decimal number D_{plim}
2: Convert $\mathbf{B}_{\text{addr}}$ into a decimal number D_{addr}
3: Convert $\mathbf{B}_{\text{pcnt}}$ into a decimal number D_{pcnt}
4: $X = \text{mod}\big(D_{\text{plim}} + f(D_{\text{addr}}, D_{\text{pcnt}}), R\big)$
5: $(k, q) = \Big(\lfloor X/Q \rfloor + \sum_{k=0}^{\lfloor X/Q \rfloor}(1 - a_k), \text{mod}(X, Q)\Big)$

A. Index Mapper

The EN converts PLIM bit sequence $\mathbf{B}_{\text{plim}}$, device address $\mathbf{B}_{\text{addr}}$, and packet counter $\mathbf{B}_{\text{pcnt}}$ to decimal numbers that are expressed as D_{plim}, D_{addr}, and D_{pcnt}, respectively. Then, the EN calculates transmission code X as

$$X = \text{mod}\big(D_{\text{plim}} + f(D_{\text{addr}}, D_{\text{pcnt}}), R\big), \tag{3}$$

where mod(m, n) represents the modulo of $m \in \mathbb{N}$ by $n \in \mathbb{N}\backslash\{0\}$, which is defined as

$$\text{mod}(m, n) = m - \left(n \times \left\lfloor \frac{m}{n} \right\rfloor\right), \tag{4}$$

where $\lfloor \cdot \rfloor$ is the floor function. Since we have $0 \leq \text{mod}(m, n) < n$, it is applicable even when m, n is negative. $f(D_{\text{addr}}, D_{\text{pcnt}})$ is an arbitrary function uniquely determined by D_{addr} and D_{pcnt}. Finally, the EN obtains transmission index (k, q) from X as

$$(k, q) = \left(\left\lfloor \frac{X}{Q} \right\rfloor + \sum_{k=0}^{\lfloor X/Q \rfloor}(1 - a_k), \text{mod}(X, Q)\right). \tag{5}$$

The EN transmits the data packet at frequency channel k and time slot q. The mapping algorithm is shown in Algorithm 1.

B. Index De-Mapper

When the GW receives a data packet at frequency channel $\tilde{k}$ and time slot $\tilde{q}$, the GW first demodulates the data packet to retrieve $\mathbf{B}_{\text{addr}}$ and $\mathbf{B}_{\text{pcnt}}$ from the packet header. Then, the GW converts them into decimal numbers, D_{addr} and D_{pcnt},

Algorithm 2 Proposed Index De-Mapper $\mathcal{F}^{-1}$

Require: $\mathcal{K}$, $\mathcal{Q}$, $\mathcal{A}$, f {Shared between EN and GW}
Require: $(\tilde{k}, \tilde{q})$ {Obtained by the GW [8]}
Require: $\mathbf{B}_{\rm addr}, \mathbf{B}_{\rm pcnt}$ {Obtained from packet header [5]}
Ensure: $\tilde{\mathbf{B}}_{\rm plim}$
1: Convert $\mathbf{B}_{\rm addr}$ into binary number $D_{\rm addr}$
2: Convert $\mathbf{B}_{\rm pcnt}$ into binary number $D_{\rm pcnt}$
3: $\tilde{X} = \left(\tilde{k} - \sum_{k=0}^{\tilde{k}}(1-a_k)\right) Q + \tilde{q}$
4: $\tilde{D}_{\rm plim} = \mathrm{mod}\Big(\tilde{X} - f(D_{\rm addr}, D_{\rm pcnt}), R\Big)$
5: Convert $\tilde{D}_{\rm plim}$ into binary number $\tilde{\mathbf{B}}_{\rm plim}$

TABLE I
EVALUATION PARAMETERS

Parameter	Value
Number of ENs N	100
Number of frequency channels K	16
Number of time slots Q	150
Payload size D	5 [byte]
Frame length $T_{\rm frame}$	60 [sec]
Number of available frequency channels $K_{\rm a}$	$\{1, 2, \ldots, 16\}$

respectively. The GW calculates received code $\tilde{X}$ as

$$\tilde{X} = \left(\tilde{k} - \sum_{k=0}^{\tilde{k}}(1-a_k)\right) Q + \tilde{q}. \tag{6}$$

Then, transmission code $\tilde{D}_{\rm plim}$ is obtained by

$$\tilde{D}_{\rm plim} = \mathrm{mod}\Big(\tilde{X} - f(D_{\rm addr}, D_{\rm pcnt}), R\Big). \tag{7}$$

In (7), divisor $\tilde{X} - f(D_{\rm addr}, D_{\rm pcnt})$ may take a negative value, but $\tilde{D}_{\rm plim}$ always takes a positive value because the modulo operation is defined by (4). Finally, $\tilde{D}_{\rm plim}$ is converted into binary number to obtain $\tilde{\mathbf{B}}_{\rm plim}$. The de-mapping algorithm is shown in Algorithm 2.

IV. PERFORMANCE EVALUATION

This section provides a numerical performance evaluation of the proposed index mapper and de-mapper. Table I shows the evaluation parameters. Without loss of generality, all ENs are assumed to generate information bit sequence randomly and transmit generated data packets at same transmission interval $T_{\rm frame} = 60$ [sec]. The following function is adopted for $f(D_{\rm addr}, D_{\rm pcnt})$:

$$f(D_{\rm addr}, D_{\rm pcnt}) = D_{\rm addr} + D_{\rm pcnt}. \tag{8}$$

Hereafter, we refer to the PLIM transmission with the proposed index mapping scheme as "PLIM w/ Proposed Mapper", the PLIM transmission without index mapping scheme as "PLIM w/o Proposed Mapper", and the conventional transmission as "w/o PLIM". Note that the performance results of the conventional scheme in [9] are equivalent to those of "PLIM w/o Proposed Mapper" due to the assumption of a generated information bit sequence.

A. Resource Usage at Each Resource

The distribution of the selected transmission indexes is evaluated by Monte Carlo simulation. We assume that the frequency channel $k = 5$ is disabled, i.e., $a_5 = 0$. Figure 2 shows the probability mass function (PMF) of the resource usage at resource number e, which is uniquely calculated as $e = k \times Q + q$. The proposed flexible index mapping scheme uniformly uses all the available resources while avoiding the resources on the disabled frequency channel $k = 5$, i.e., $750 \le e < 900$. On the other hand, the conventional mapping scheme [9] cannot utilize frequency channels $k \ge \lfloor \log_2 K_{\rm a} \rfloor + \sum_{k=0}^{\lfloor \log_2 K_{\rm a} \rfloor}(1-a_k)$ and time slots $q \ge \lfloor \log_2 Q \rfloor$.

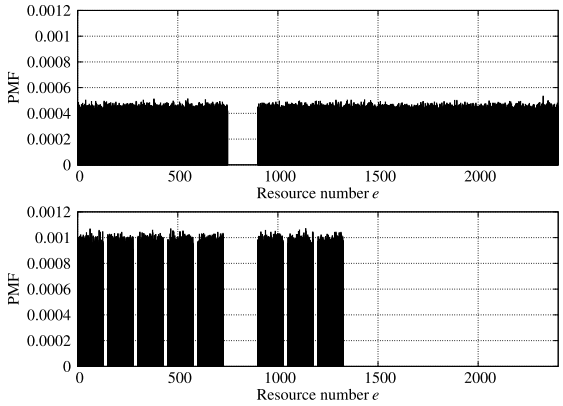

Fig. 2. Resource usage (top: PLIM w/ Proposed Mapper, bottom: PLIM w/o Proposed Mapper).

B. Throughput Performance

The theoretical throughput, S [bps], can be calculated as

$$S = \left(1 - \frac{1}{R}\right)^{N-1} \times \left(B_{\rm pl} + B_{\rm plim}\right) \times \frac{1}{T_{\rm frame}}, \tag{9}$$

where N is the number of ENs. In (9), the first term is the probability of successful packet transmission, the second term is the data size per packet, and the third term is the inverse of the transmission interval. The parameters R and $B_{\rm plim}$ are expressed as

$$R = \begin{cases} K_{\rm a} \times Q & \text{w/ Proposed Mapper} \\ 2^{\lfloor \log_2 K_{\rm a} \rfloor + \lfloor \log_2 Q \rfloor} & \text{w/o Proposed Mapper,} \end{cases} \tag{10}$$

$$B_{\rm plim} = \begin{cases} \lfloor \log_2 R \rfloor & \text{w/ PLIM} \\ 0 & \text{w/o PLIM.} \end{cases} \tag{11}$$

In (10), the proposed mapper uses $K_{\rm a}$ frequency channels and Q time slots. On the other hand, the conventional mapper uses $2^{\lfloor \log_2 K_{\rm a} \rfloor}$ frequency channels and $2^{\lfloor \log_2 Q \rfloor}$ time slots due to the constraint of the number of available resources. Note that in the case of "w/o PLIM", number of available resources R is equivalent to the case of "PLIM w/ Proposed Mapper", i.e., $R = K_{\rm a} \times Q$.

Figure 3 shows throughput S [bps] as a function of number of available frequency channels $K_{\rm a}$. The PLIM transmission improves the throughput performance compared to the conventional LoRaWAN due to the information-bearing index. The proposed index mapper further improves the throughput performance because of two factors. The first factor is reduced packet collisions due to mapping the information-bearing index to all the available frequency channels and time slots. The second factor is the increased number of information bits conveyed by the index by jointly assigning

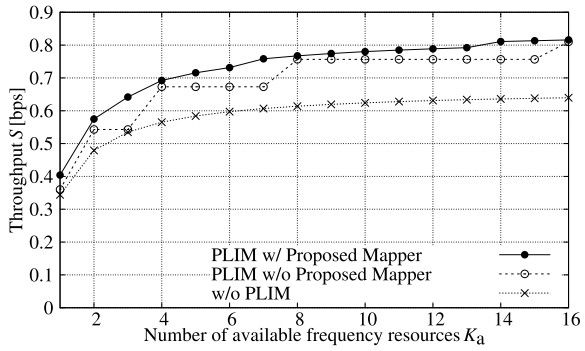

Fig. 3. Theoretical throughput S versus number of available frequency channels $K_{\rm a}$.

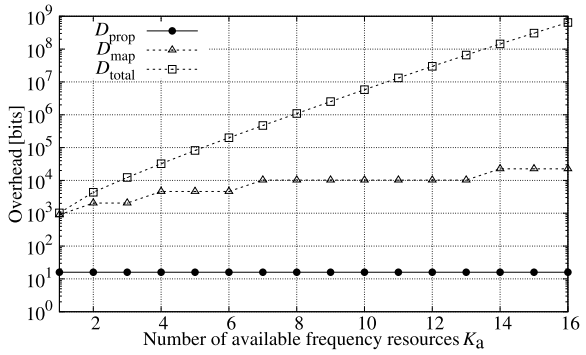

Fig. 4. Overhead $D_{\rm prop}$ (w/ Proposed Mapper), $D_{\rm map}$ (w/o Proposed Mapper, map exchange), and $D_{\rm total}$ (w/o Proposed Mapper, all map store) versus number of available frequency channels $K_{\rm a}$.

the index to frequency channels and time slots. In particular, the throughput improves about 1.18 times when $K_{\rm a} = 3$ ($K_{\rm a} \times Q - 2^{\lfloor \log_2 K_{\rm a} \rfloor + \lfloor \log_2 Q \rfloor} > 0$). On the other hand, when $K_{\rm a}$ is the power of 2, the conventional mapper can use the all available frequency channels. Thus the difference becomes smaller.

C. Required Memory Size

Next, we show how the proposed index mapping can reduce the memory size at EN and GW required for the PLIM operation. Since the proposed scheme requires the available frequency channel set only, which is obtained as a bitmap from the GW [5], the memory size, $D_{\rm prop}(K)$, required for the proposed scheme is expressed as

$$D_{\rm prop}(K) = K. \tag{12}$$

On the other hand, if the proposed index mapping scheme is not adopted, a specific index map needs to be exchanged every resource update when the frequency channel allocation changes due to the environment change. If the index map is exchanged at every resource update, the required memory size for an index map, $D_{\rm map}(K_{\rm a}, Q)$, becomes

$$D_{\rm map}(K_{\rm a}, Q) = R_{\rm rec}(K_{\rm a}, Q) \times D_{\rm rec}(K_{\rm a}, Q), \tag{13}$$

where $R_{\rm rec}(K_{\rm a}, Q)$ is the number of bits to indicate the indexes and $D_{\rm rec}(K_{\rm a}, Q)$ is the required memory size per index, which are defined as

$$\begin{cases} R_{\rm rec}(K_{\rm a}, Q) \triangleq 2^{\lfloor \log_2 (K_{\rm a} \times Q) \rfloor} \\ D_{\rm rec}(K_{\rm a}, Q) \triangleq \lceil \log_2 (K_{\rm a} \cdot Q) \rceil \end{cases}, \tag{14}$$

where $\lceil \cdot \rceil$ denotes the ceiling function. If all index maps are stored at the EN and the GW in advance to avoid the resource map exchange, the memory size of $D_{\rm total}(K_{\rm a}, Q)$ is required, which is calculated as

$$D_{\rm total}(K, Q) = \sum_{K_{\rm a}=1}^{K} \left({}_K{\rm C}_{K_{\rm a}} \times D_{\rm map}(K_{\rm a}, Q) \right), \tag{15}$$

where ${}_m{\rm C}_n$ denotes the binomial coefficient.

Figure 4 shows $D_{\rm map}$, $D_{\rm total}$, and $D_{\rm prop}$ as a function of number of available frequency channels $K_{\rm a}$. The proposed scheme can significantly reduce the memory size compared to the conventional schemes. In particular, the memory size can be reduced by 1/640 (compared to the map exchange) and 1/68224 (compared to all maps store) for $K_{\rm a} = 8$.

V. Conclusion

This letter proposed an index mapping scheme for packet-level index modulation (PLIM) to further improve its throughput performance. The conventional PLIM transmission could not fully utilize the available frequency and time resources. The proposed index mapping fully utilizes the available frequency channels and time slots to avoid packet collisions through simple index mapping and de-mapping. The proposed mapping does not require any information exchange between EN and GW except for the frequency channel allocation, which is currently available in LoRaWAN by default. Theoretical performance evaluation has shown that the proposed scheme improves the throughput performance by about 18% compared to the original PLIM transmission and significantly reduces overhead.

References

[1] K. Mekki, E. Bajic, F. Chaxel, and F. Meyer, "A comparative study of LPWAN technologies for large-scale IoT deployment," *ICT Exp.*, vol. 5, no. 1, pp. 1–7, Mar. 2019.

[2] H. Wang and A. O. Fapojuwo, "A survey of enabling technologies of low power and long range machine-to-machine communications," *IEEE Commun. Surveys Tuts.*, vol. 19, no. 4, pp. 2621–2639, 4th Quart., 2017.

[3] A. Lavric and V. Popa, "Internet of Things and LoRa low-power wide-area networks: A survey," in *Proc. 2017 Int. Symp. Signals Circuits Syst. (ISSCS)*, Jul. 2017, pp. 1–5.

[4] U. Raza, P. Kulkarni, and M. Sooriyabandara, "Low power wide area networks: An overview," *IEEE Commun. Surveys Tuts.*, vol. 19, no. 2, pp. 855–873, 2nd Quart., 2017.

[5] "LoRaWAN 1.1 Specification." LoRa Alliance Technical Committee. [Online]. Available: https://lora-alliance.org/wp-content/uploads/2020/11/lorawantm_specification_-v1.1.pdf (accessed: Sep. 1, 2021).

[6] J. P. S. Sundaram, W. Du, and Z. Zhao, "A survey on LoRa networking: Research problems, current solutions, and open issues," *IEEE Commun. Surveys Tuts.*, vol. 22, no. 1, pp. 371–388, 1st Quart., 2020.

[7] T. Mao, Q. Wang, Z. Wang, and S. Chen, "Novel index modulation techniques: A survey," *IEEE Commun. Surveys Tuts.*, vol. 21, no. 1, pp. 315–348, 1st Quart., 2019.

[8] K. Adachi, K. Tsurumi, A. Kaburaki, O. Takyu, M. Ohta, and T. Fujii, "Packet-level index modulation for LoRaWAN," *IEEE Access*, vol. 9, pp. 12601–12610, 2021.

[9] M. Ohta and T. Fujii, "Intra-system interference avoidance for packet-level index modulation in Internet of Things, " in *Proc. Asia–Pac. Signal Inf. Process. Assoc. Annu. Summit Conf. (APSIPA)*, 2021, pp. 1958–1962.