Simple Clock Drift Estimation and Compensation for Packet-Level Index Modulation and Its Implementation in LoRaWAN

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***Abstract*—Low-power wide-area network (LPWAN), which includes the long-range wide-area network (LoRaWAN) protocol, is an enabling technology that satisfy low power consumption and long-range communication. In many applications of LPWAN, an end node (EN) transmits data at regular intervals. Based on this, we had previously proposed the concept of packet-level index modulation (PLIM) to increase the number of information bits transmitted by one data packet. In PLIM, the generation interval between two consecutive packets is split into multiple time slots. Each EN transmits its packet in a specific combination of time slot and frequency channel, which represents the index, to convey additional information bits. To retrieve additional information, the gateway (GW) detects the time slot in which the data packet is being transmitted. Therefore, accurate synchronization between EN and GW is essential. However, clock drift occurs due to the inexpensive real-time clock oscillator on each EN, which results in timing misalignment between each node and the GW. This article proposes a simple clock drift estimation and compensation method for the PLIM. An experimental measurement is performed to model the clock drift. The numerical results obtained using the clock drift model show that it can accurately detect the time slot index under the influence of clock drift. Furthermore, PLIM is implemented on a commercial LoRaWAN node and GW to demonstrate its practicability.**

***Index Terms*—Clock drift, implementation, index modulation, long-range wide-area network (LoRaWAN), LPWA.**

I. Introduction

THE Internet of Things (IoT) technology has been applied in various domains [1]. In an IoT system, it is critical to achieve long-range communication and low energy consumption [2]. A low-power wide-area network (LPWAN), which includes a long-range wide-area network (LoRaWAN), is a key enabler for such requirements [3]. LoRaWAN has gained considerable attention owing to its operability in an unlicensed band and low deployment cost. LoRaWAN adopts a chirp spread spectrum (CSS) modulation, and realizes long-distance communication [4]. In LoRaWAN, each end node (EN) selects one of the preassigned frequency channels and transmits a data packet in an ALOHA-based protocol without carrier sensing (CS) of the channel occupancy, except for some countries.[1]

In many wireless sensor networks (WSNs), an EN periodically transmits data packets to a gateway (GW). The duty cycle (DC), which is a critical capacity limitation factor, defines the ratio of transmission time to packet generation interval. Owing to the DC restriction, an EN cannot transmit a packet immediately after another. Because there are functional and battery capacity limitations in LoRaWAN EN, it is not practical to implement a complicated method to improve the capacity.

A. Motivation

There are numerous techniques to increase the capacity of LoRaWAN by appropriately setting parameters such as a spreading factor (SF) and allocating radio resources such as the frequency channel [7]–[14]. The concept of packet-level index modulation (PLIM) is proposed for LoRaWAN in [15]. PLIM takes advantage of the fact that the generation interval of consecutive data packets transmitted by each EN, called the *frame*, is typically long in LoRaWAN. The generation interval is split into multiple time slots. Each EN determines the time slot and the frequency channel on which it transmits a packet. The combination of the time slot and frequency channel, which represents an *index*, conveys additional information. The GW can directly obtain the frequency channel index once a data packet is received on a specific frequency channel. Then, the GW detects the time slot in which an EN transmits a packet and retrieves the additional information bits conveyed by the index. Therefore, stringent frame synchronization is necessary between the GW and each EN. However, the frame synchronization between the GW and each EN may be lost due to the delay between packet transmission and reception [16], [17], and timing misalignment between the EN and GW, called *clock drift* [18]. These factors reduce the accuracy of time slot

Manuscript received 27 July 2021; revised 30 November 2021; accepted 19 January 2022. Date of publication 3 February 2022; date of current version 8 August 2022. This work was supported by the Ministry of Internal Affairs and Communications under Grant MIC/SCOPE JP205004001. *(Corresponding author: Kohei Tsurumi.)*

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Digital Object Identifier 10.1109/JIOT.2022.3148767

[1] All ENs operating in Japan must perform listen-before-talk (LBT) based on ARIB STD-T108 regulations [5], [6].

index detection. In [16], the transmission delay was analyzed for slotted ALOHA in LoRaWAN. The simulation results indicated that the transmission delay for different payload sizes is in the range of milliseconds, which significantly decreases with lower SF. In [17], the latency was considered in a fog-based architecture where GW is associated with two separated network servers. The fog architecture reduces the end-to-end latency. Because the target of this study is a scenario in which an EN periodically transmits data packets to a GW and the GW performs time slot detection, no significant delay occurs between the packet transmission and reception. Therefore, we focused only on the clock drift and proposed a simple clock drift estimation and compensation method for time slot index detection in PLIM based on that observation.

B. Related Works

Because most studies addressing the timing synchronization issue in WSN generally assume that the clock skew is constant over a long period, they use the terms "clock skew" and "clock drift" interchangeably [19]. The impact of clock drift in LoRaWAN has been described in several studies. It has been shown that temperature change [20], [21] and aging [22] influence the clock drift. In [20], the crystal oscillator had ± 20 ppm at 25 °c, which remained constant over temperature. It has been shown that temperature, humidity, pressure, and orientation influence the clock drift [21]. Quartz crystals have the highest sensitivity to drastic changes in temperature and present a parabolic frequency dependence over time given by $\Delta f/f_0 = \beta(T - T_0)^2$, where β is a temperature coefficient, f_0 is the clock's nominal value, Δf is the difference between clock's frequency and f_0, and T_0 is the turnover temperature in the range 25 ± 5 °c. The frequency shift also causes clock drift. The relation between frequency shift and time for a quartz crystal oscillator is logarithmic. In [22], it was explained that the effects of both ageing and temperature can be considered with the Arrhenius model or empirical model called Mattuschka model. If there is a clock drift, the synchronization between two clocks deteriorates as time elapses. The most common approach to address clock drift is to perform synchronization using a downlink signal. In [23], an EN updated its local real-time clock (RTC), following a synchronization message broadcast received from a GW. If the difference between the local timestamp obtained by the RTC and the timestamp retrieved from the synchronization message is larger than a predetermined margin, the EN updates its RTC; otherwise, it performs self-calibration. In [24], once the GW receives a packet from an EN, it sets its timestamp and sends it back to the EN. Simultaneously, the EN sets its timestamp once it completes packet transmission. Calculating a difference between the timestamp transmitted from the GW and its timestamp enables the EN to estimate the delay offset. The EN adds a delay to its local RTC to update it. In [25], a time slotted (TS)-LoRa utilizing flexible guard time was introduced, and its network capacity was analyzed. For synchronization and acknowledgment (ACK) among the ENs, a synchronization ACK (SACK) signal is transmitted at the frame end. In another study [20], when one EN broadcasts a ping message for synchronization, the other ENs receive the ping message and check the waiting time before the neighbor's transmission is received. Linear regression was used in another study to compensate for clock skew [26]. Another study used an out-of-band communication, such as a global positioning system (GPS), radio-controlled clocks (RCCs), or a frequency modulation radio data system (FM-RDS) to provide the required time dissemination [27]. Additionally, a new hardware architecture design method called the hardware interruption cross-layer (HICL) algorithm was proposed [28]. Based on this architecture, a beacon transmission delay calculation was performed, and a synchronization compensation method was implemented. Haxhibeqiri *et al.* [18] proposed a low-overhead scheduling algorithm. Recently, they performed experimental measurements to show the impact of clock drift on the scheduling algorithm and demonstrated the possibility of practical implementation [21].

C. Objective and Main Contributions of This Article

The primary objective of the studies [18]–[28] was to synchronize *the clocks of ENs* for the time-domain scheduling of multiple ENs. Hence, the synchronization signal transmitted from the GW had to be used for clock drift correction and synchronization between ENs. The existing literature considers a synchronized system that requires ENs to synchronize with each other [21], [23]. Thus, the existing works focused on synchronizing multiple ENs by compensating the clock drifts that are different among ENs. In this study, unlike that in related works, there is no aim to synchronize the ENs to avoid centralized control and information exchange for a synchronization signal that uses a limited radio resource. Although no synchronization is necessary between LoRaWAN ENs, stringent synchronization between *each LoRaWAN EN and the GW* is essential for accurately detecting the time slot index in PLIM.

The clock at the GW is considered as the reference clock. Even when multiple ENs are communicating with a GW, the clock drift of EN can be treated independently from the other ENs, as no synchronization between ENs is required. Therefore, this article focuses on a specific EN and GW without loss of generality. Furthermore, the objective of this study is not to synchronize an EN and the GW by centralized control but to compensate for the synchronization error at GW caused by the clock drift between an EN and the GW. Thus, the proposed approach does not require any information exchange between the EN and GW. The GW performs the entire operation for compensation. Thus, no additional burden will be introduced to the ENs, which is a significant advantage in LoRaWAN, where each EN is relatively cheap and computationally weak. In practice, it is crucial that a synchronization method can be easily implemented. In [28], synchronization was achieved using a Class B beacon signal, which means that this system cannot accommodate Class A devices. In contrast, this article proposes a simple clock drift estimation and compensation method that does not require additional communication overhead and computation at the ENs. Because the proposed method utilizes only the basic functionality of

LoRaWAN, it can be implemented in any LoRaWAN system by modifying the packet reception algorithm at the GW. The procedure of time slot detection is as follows. At the first and second transmission, EN transmits the confirmed message at a certain time slot and frequency channel. Because EN and GW have common data for clock drift estimation, i.e., transmission interval, time slot length, and transmission timing offset, GW can estimate clock drift. In the subsequent packet reception, GW detects the time slot index based on the estimated clock drift. In addition, at each packet reception, GW updates the clock drift. In this way, GW detects the time slot index according to PLIM's inherent method. We confirm that the proposed method can compensate for the clock drift and detect time slot index through simulations and an experiment on real hardware. We implement PLIM on real hardware, i.e., in LoRaWAN EN and GW with Arduino. The experimental results show that PLIM with the proposed clock drift estimation and compensation method works accurately.

The primary contributions of this study can be summarized as follows.

1) The clock misalignment between EN and the GW per unit time is measured, and the mean and variance are derived to model the clock drift.
2) A simple yet effective clock drift estimation and compensation scheme is proposed. The algorithm is implemented at the GW, and it does not introduce any additional complexity to the ENs, except for a fixed transmission timing offset.
3) PLIM [15] and the proposed clock drift estimation and compensation scheme are implemented on commercially available LoRaWAN GW and ENs to demonstrate its practicability. Both computer simulations and experimental evaluations demonstrate the effectiveness of the proposed scheme.
4) Subsequently, the simulation is expanded to multiple ENs to analyze the impact of packet collision on the misdetection probability.

D. Organization

The remainder of this article is organized as follows. Section II describes the PLIM system and the impact of clock drift. Section III explains the measurement of clock drift using a commercial LoRaWAN GW and ENs for clock drift modeling, which is important for developing the proposed clock drift estimation and compensation scheme. Section IV explains the clock drift estimation and compensation operations at GW and ENs. Section V compares the simulation and experimental results. Finally, Section VI concludes this article.

II. LoRaWAN With Packet-Level Index Modulation

A. Operation Principle of PLIM

This article considers one pair of a GW and an EN without loss of generality and focuses on the packet transmission and reception of arbitrary data packets i (≥ 0).

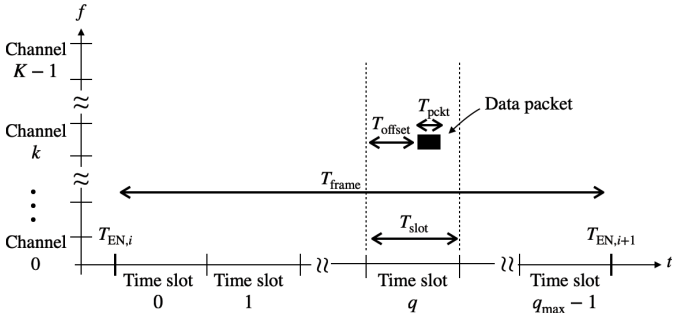


Fig. 1. Concept of PLIM.

Data packets are generated every T_{frame} [s]. There are K frequency channels, and the EN selects one frequency channel for packet transmission. The EN splits the generation interval T_{frame}, between periodically generated data packets, into multiple time slots, as shown in Fig. 1 [15]. Note that PLIM does not require synchronization between ENs. T_{slot} [s] denotes the time slot length. Accordingly, the number of available time slots is

$$q_{\max} = \left\lfloor \frac{T_{\text{frame}}}{T_{\text{slot}}} \right\rfloor \tag{1}$$

where $\lfloor \cdot \rfloor$ returns the largest integer smaller than or equal to the argument. The time slot length T_{slot} is expressed as

$$T_{\text{slot}} = \alpha \times T_{\text{pckt}} \tag{2}$$

where α (≥ 1) represents a time slot scaling factor [15], and T_{pckt} [s] represents the packet length, including the preamble symbols, CSS-modulated overhead, and payload data.

1) At Transmitting EN: Each EN selects a specific combination of the time slot and frequency channel, that is, *index*, for packet transmission. The EN splits the data sequence $\mathbf{B}_i \in \{0,1\}^{(\lfloor \log_2(K \times q_{\max}) \rfloor + B_{\text{pl}}) \times 1}$ into two sequences $\mathbf{B}_{\text{pckt},i} \in \{0,1\}^{B_{\text{pl}} \times 1}$ and $\mathbf{B}_{\text{plim},i} \in \{0,1\}^{\lfloor \log_2(K \times q_{\max}) \rfloor \times 1}$. The data sequence $\mathbf{B}_{\text{pckt},i}$ is CSS-modulated into multiple data symbols that are transmitted by data packet i. The EN determines the time slot q_i and frequency channel k_i based on $\mathbf{B}_{\text{plim},i}$ as

$$(k_i, q_i) = \mathcal{F}\left(\mathbf{B}_{\text{plim},i}\right) \tag{3}$$

where $\mathcal{F}$ denotes an arbitrary mapping function from the data sequence $\mathbf{B}_{\text{plim},i}$ to index (k_i, q_i).

In PLIM, the EN can transmit an additional $|\mathbf{B}_{\text{plim},i}|$ at each data packet, which is given by [15]

$$|\mathbf{B}_{\text{plim},i}| = \left\lfloor \log_2(K \times q_{\max}) \right\rfloor. \tag{4}$$

The EN transmits CSS-modulated data packet i containing the data sequence $\mathbf{B}_{\text{pckt},i}$ on the frequency channel k_i at the following timing:

$$t_{\text{EN},i} = \underbrace{T_{\text{EN},0} + (i \times T_{\text{frame}})}_{\triangleq T_{\text{EN},i}} + (q_i \times T_{\text{slot}}) \tag{5}$$

where $T_{\text{EN},0}$ [s] denotes the starting time of the first frame at EN. For the initial synchronization between each EN and the GW, each EN transmits the first packet at time slot Q_0. This packet is shared between the GW and the EN in advance.

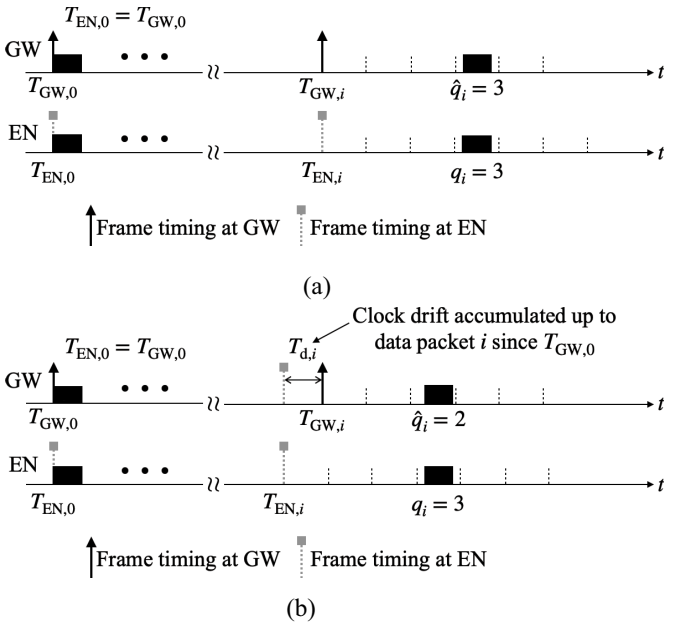


Fig. 2. Index misdetection due to clock drift when $T_{\mathrm{d},i} < 0$. (a) Without clock drift. (b) With clock drift.

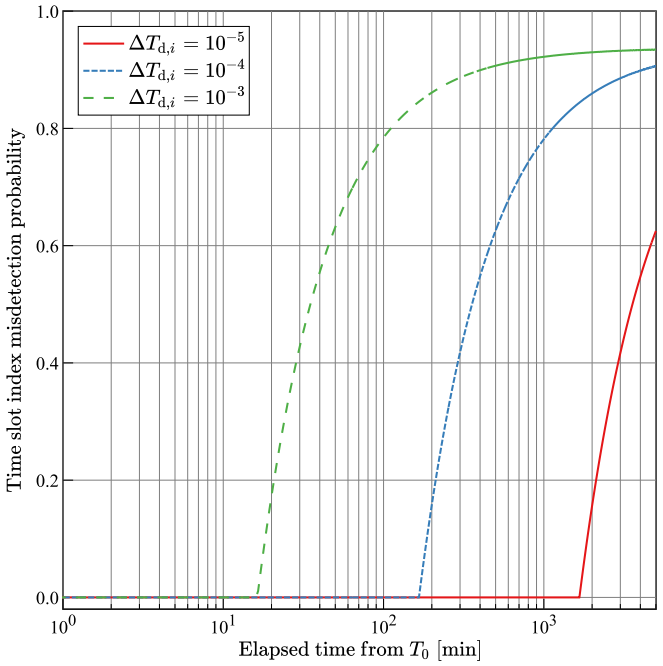


Fig. 3. Impact of clock drift on misdetection probability of time slot index.

The value of Q_0 can be either randomly assigned to each EN or determined based on the identification (ID) of each EN. The GW can set $T_{\mathrm{GW},0} = T_{\mathrm{EN},0}$ based on this initial synchronization.

2) At Receiving GW: Upon receiving data packet i at time $t_{\mathrm{GW},i}$ on the frequency channel k_i, the GW detects the time slot index as [15]

$$\hat{q}_i = \max\left(0, \min\left(q_{\max} - 1, \left\lfloor \frac{(t_{\mathrm{GW},i} - T_{\mathrm{GW},i})}{T_{\mathrm{slot}}} \right\rfloor\right)\right) \quad (6)$$

where $\max(,)$ and $\min(,)$ return the larger and smaller values of the arguments, respectively; $T_{\mathrm{GW},i}$ denotes the starting timing of frame i, which is calculated as

$$T_{\mathrm{GW},i} = T_{\mathrm{GW},0} + i \times T_{\mathrm{frame}}. \quad (7)$$

Thereafter, the GW retrieves the transmitted data sequence as follows:

$$\hat{\mathbf{B}}_{\mathrm{plim},i} = \mathcal{F}^{-1}(k_i, \hat{q}_i) \quad (8)$$

where $\mathcal{F}^{-1}$ denotes the inverse mapping function.

B. Impact of Clock Drift on Time Slot Detection

A time slot index detection error occurs when the frame synchronization between an EN and the GW is lost owing to clock drift, that is, $T_{\mathrm{GW},i} \neq T_{\mathrm{EN},i}$. In this study, clock drift was defined as the *relative* difference between the clocks at the GW and each EN. The clock at the GW is considered as the reference clock. Fig. 2 demonstrates how the clock drift impacts the time slot index detection. Although the GW and EN are synchronized at the first packet, that is, $T_{\mathrm{GW},0} = T_{\mathrm{EN},0}$, the synchronization deteriorates over time. In an ideal case, the transmission timing of data packet i transmitted in time slot q_i is expressed as in (5). However, if clock drift exists, the transmission timing at GW can be expressed as

$$\begin{aligned} t_{\mathrm{EN},i} &= T_{\mathrm{EN},0} + (i \times T_{\mathrm{frame}}) + (q_i \times T_{\mathrm{slot}}) \\ &= T_{\mathrm{GW},0} + (i \times T_{\mathrm{frame}}) + (q_i \times T_{\mathrm{slot}}) + \underbrace{\int_{T_{\mathrm{GW},0}}^{t_{\mathrm{GW},i}} \Delta T_{\mathrm{d}}(t)dt}_{\triangleq T_{\mathrm{d},i}} \\ &= T_{\mathrm{GW},i} + (q_i \times T_{\mathrm{slot}}) + T_{\mathrm{d},i} \end{aligned} \quad (9)$$

where $\Delta T_{\mathrm{d}}(t)$ represents the relative clock drift between the EN and GW at time t, and $T_{\mathrm{d},i}$ represents the accumulated relative clock drift until data packet i.

Fig. 3 shows the impact of the clock drift on the misdetection probability of the time slot index. $T_{\mathrm{frame}} = 30$ [s] and $T_{\mathrm{slot}} = 1$ [s] are set, and $\Delta T_{\mathrm{d}}(t) = \Delta T_{\mathrm{d}}$ is assumed for simplicity. We can observe that without addressing the clock drift, the misdetection probability of the time slot index increases as time elapses from $T_0 = T_{\mathrm{GW},0}$. Therefore, clock drift compensation must be considered based on the limited capability of the ENs. Thus, this article proposes a simple clock drift estimation and compensation algorithm performed at the GW.

III. Clock Drift Modeling Through Experimental Measurement

Experimental measurements were performed to model the clock drift using commercially available LoRaWAN GW (Dragino LG-01 [29]) and ENs (LoRa Mini Dev-JP) in an indoor environment. Table I lists the experimental parameters [5], [13], [15], [30], [31].

The normalized clock drift, which is the clock drift per unit time, is defined as

$$\Delta T_{\mathrm{d},i} \triangleq \frac{\left((T_{\mathrm{GW},i} - T_{\mathrm{GW},i-1}) - T_{\mathrm{frame}}\right)}{T_{\mathrm{frame}}} \quad \forall i > 0 \quad (10)$$

where $T_{\mathrm{GW},i}$ is the time when the GW receives packet i that is periodically transmitted by the EN every T_{frame} [s].

TABLE I
EXPERIMENTAL SETUP

Parameter	Value
Carrier frequency f_c	924.0 & 924.2 [MHz]
Bandwidth W	125 [kHz]
Packet generation interval T_{frame}	100 [s]
Time slot length T_{slot}	1 [s]
Spreading factor S	10
CS level	−80 [dBm]
CS duration	5 [ms]

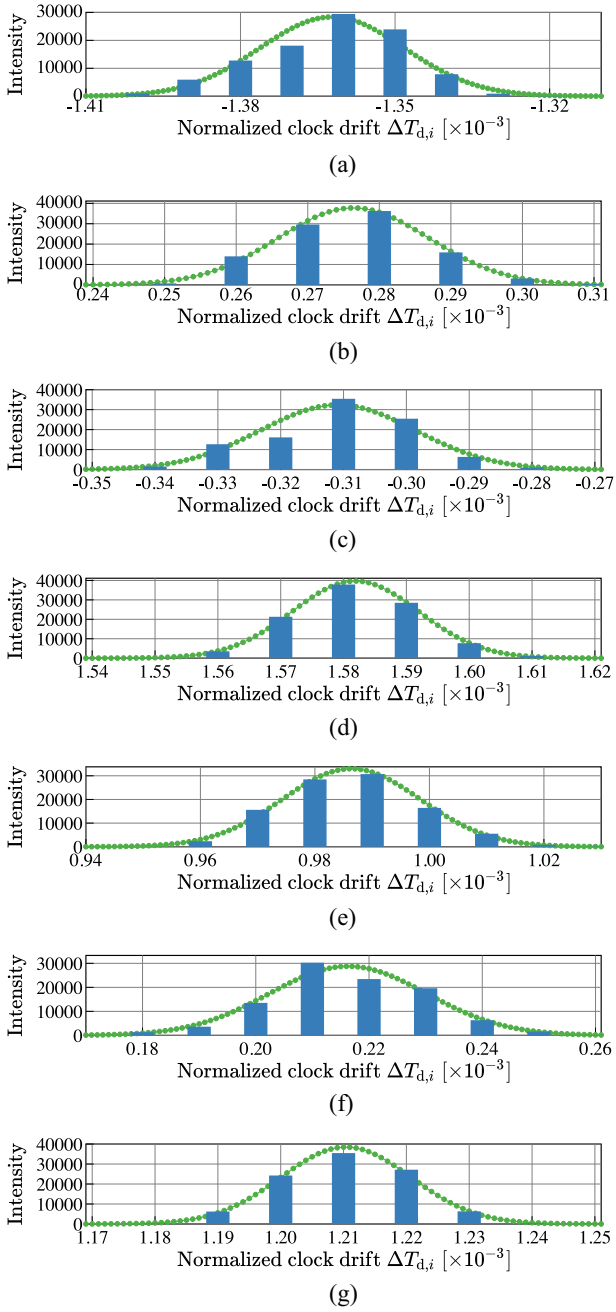


Fig. 4. Measurement results of relative clock drift between Dragino LG-01 and LoRa Mini Dev-JP. (a) EN 1. (b) EN 2. (c) EN 3. (d) EN 4. (e) EN 5. (f) EN 6. (g) EN 7.

If there is no clock drift, then $\Delta T_{\text{d},i} = 0$. In the measurement, $T_{\text{frame}} = 100$ [s] is set. The histograms of the experimentally obtained $\Delta T_{\text{d},i}$ are presented in Fig. 4. The normalized clock drift $\Delta T_{\text{d},i}$ can be approximately modeled using a normal distribution.

TABLE II
MEAN AND VARIANCE OF NORMALIZED CLOCK DRIFT

	p value	Mean value μ [s]	Variance σ^2 [s^2]
EN 1	0.0214	-1.36×10^{-3}	1.98×10^{-10}
EN 2	0.68	0.28×10^{-3}	1.12×10^{-10}
EN 3	0.701	-1.91×10^{-3}	1.76×10^{-10}
EN 4	0.25	-6.56×10^{-4}	9.59×10^{-11}
EN 5	0.0156	-1.40×10^{-3}	3.19×10^{-10}
EN 6	0.892	-2.99×10^{-5}	1.27×10^{-10}
EN 7	0.041	-4.10×10^{-4}	1.09×10^{-10}

The Kolmogorov–Smirnov test, which is a null test used to compare the empirical distribution with the reference cumulative distribution, was conducted to verify the validity of modeling the normalized clock drift by using a normal distribution [32]. Considering $(\Delta T_{\text{d},1}, \ldots, \Delta T_{\text{d},i}, \ldots, \Delta T_{\text{d},I})$ for I samples, the empirical distribution function $\hat{F}_I$ is defined as

$$\hat{F}_I(x) \triangleq \frac{1}{I} \sum_{i=1}^{I} \mathbf{1}\left(\Delta T_{\text{d},i} \leq x\right) \tag{11}$$

where $\mathbf{1}(A)$ is the indicator function of event A. The Kolmogorov–Smirnov statistic d_I is the absolute maximum deviation between the theoretical distribution $F(x)$ and the empirical distribution $\hat{F}_I(x)$, which is expressed as

$$\mathrm{d}_I = \sup_x \left| \hat{F}_I(x) - F(x) \right| \tag{12}$$

where $\sup_x$ denotes the supreme of the set of distances. Because the sample data were rounded to only a few integers due to the limitations of the measurement campaign, an accurate result cannot be obtained. Hence, random noise was added to these sample data to obtain an approximation result. The quantization noise was modeled as a uniform distribution. Based on h, which denotes the bin width of the histogram, it is sufficient to add random noise from the distribution $\mathrm{Unif}[-h/2, h/2]$ [33].

The p value indicates the probability of the occurrence of an observed difference. In this study, p values less than 0.01 were considered statistically significant. The p values of the ENs listed in Table II do not disprove the null hypothesis, indicating that the empirical distribution agrees well with the reference cumulative distribution.

Therefore, $\Delta T_{\text{d},i}$ can be modeled as a Gaussian random variable following $\mathcal{N}(\mu, \sigma^2)$, with:

$$\begin{cases} \mu = \frac{1}{I} \sum_{i=1}^{I} \Delta T_{\text{d},i} \\ \sigma^2 = \frac{1}{I} \sum_{i=1}^{I} \left(\Delta T_{\text{d},i} - \mu\right)^2. \end{cases} \tag{13}$$

Table II lists the values of μ and σ^2 for the different EN values.

Thus, the *relative* clock drift accumulated until data packet i can be modeled as

$$T_{\text{d},i} = T_{\text{d},i-1} + \int_{(i-1)\times T_{\text{frame}}}^{i \times T_{\text{frame}}} \Delta T_{\text{d}}(t) dt \quad \forall i > 0 \tag{14}$$

where $T_{\text{d},0} = 0$ and $\Delta T_{\text{d}}(t) \sim \mathcal{N}(\mu, \sigma^2)$.

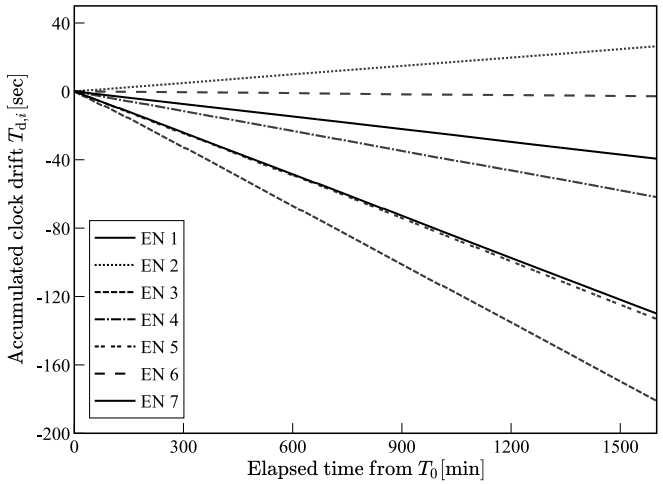


Fig. 5. Accumulated clock drift of seven ENs as a function of the elapsed time from T_0.

Fig. 5 shows the accumulated relative clock drift $T_{\mathrm{d},i}$ with respect to the elapsed time from $T_{\mathrm{GW},0} = T_{\mathrm{EN},0} = T_0$. As depicted in the figure, $T_{\mathrm{d},i}$ either increases or decreases almost linearly. This result is consistent with those of existing studies [21]. Accordingly, we introduced a simple yet effective clock drift estimation and compensation scheme at the GW.

IV. Time Slot Estimation With Clock Drift Estimation and Compensation

As described in Section II-B, the clock drift significantly reduces the accuracy of the time slot index detection. Many studies have attempted to synchronize the GW and ENs [18]–[28]. However, considering simple ENs, complicated synchronization may not be implementable. Thus, we propose a time slot index detection method that compensates for the impact of the clock drift at the GW itself.

A. Operation at Transmitting EN

The EN transmits data packet i at

$$t_{\mathrm{EN},i} = T_{\mathrm{EN},0} + (i \times T_{\mathrm{frame}}) + (q_i \times T_{\mathrm{slot}}) + T_{\mathrm{offset}} \quad (15)$$

where T_{offset} [s] denotes the transmission timing offset from the starting time of each time slot to absorb the impact of the small clock drift.

B. Operation at Receiving GW

The GW estimates clock drift in a recursive manner. Fig. 6 presents the flowchart of the proposed clock drift estimation and compensation method when the GW receives data packet i. Considering the clock drift estimate $\hat{T}_{\mathrm{d},j}$ on the reception of data packet j ($j < i$), the GW calculates the additional clock drift $\hat{T}_{\mathrm{c},i}$, which occurs between data packets j and i, as follows:

$$\hat{T}_{\mathrm{c},i} = \left(\frac{\hat{T}_{\mathrm{d},j}}{t_{\mathrm{GW},j} - T_{\mathrm{GW},0}}\right) \times \left(t_{\mathrm{GW},i} - t_{\mathrm{GW},j}\right). \quad (16)$$

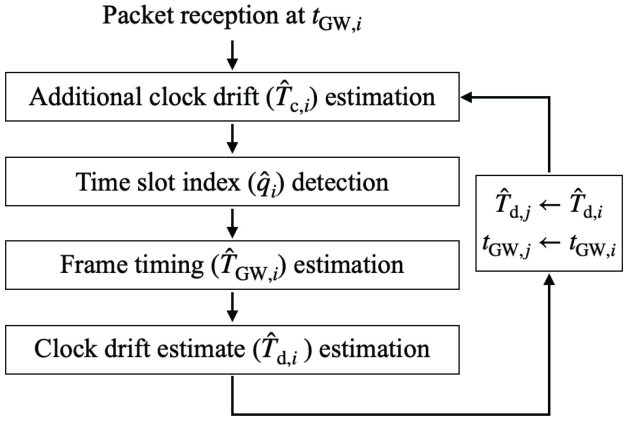


Fig. 6. Flowchart of clock drift estimation and compensation at GW.

The GW detects the time slot index by compensating for the clock drift as

$$\hat{q}_i = \max\left(0, \min\left(q_{\max} - 1, \left\lfloor \frac{\left(t_{\mathrm{GW},i} - \hat{T}_{\mathrm{GW},i} - \left(\hat{T}_{\mathrm{d},j} + \hat{T}_{\mathrm{c},i}\right)\right)}{T_{\mathrm{slot}}} \right\rfloor\right)\right). \quad (17)$$

Once the time slot index estimate $\hat{q}_i$ is obtained, the start timing of frame i is calculated as

$$\hat{T}_{\mathrm{GW},i} = t_{\mathrm{GW},i} - \left(\hat{q}_i \times T_{\mathrm{slot}}\right) - T_{\mathrm{offset}}. \quad (18)$$

Subsequently, the GW updates the clock drift estimate $\hat{T}_{\mathrm{d},i}$ as

$$\hat{T}_{\mathrm{d},i} = \hat{T}_{\mathrm{d},j} + \left\{\left(\hat{T}_{\mathrm{GW},i} - \hat{T}_{\mathrm{GW},j}\right) - (i-j) \times T_{\mathrm{frame}}\right\}. \quad (19)$$

The first and second packets are always transmitted in predetermined time slots, that is, $q_0 = Q_0$ and $q_1 = Q_1$, to improve the clock drift estimation accuracy. The values of Q_0 and Q_1 can be randomly assigned to each EN or determined based on each the ID of each EN. Once the GW receives the first and second packets, the GW calculates the initial clock drift value as

$$\hat{T}_{\mathrm{d},1} = \underbrace{\left(t_{\mathrm{GW},1} - Q_1 \times T_{\mathrm{slot}}\right)}_{T_{\mathrm{GW},1}} - \underbrace{\left(t_{\mathrm{GW},0} - Q_0 \times T_{\mathrm{slot}}\right)}_{T_{\mathrm{GW},0}} - T_{\mathrm{frame}}. \quad (20)$$

Fig. 7 illustrates the operation of the proposed clock drift compensation. The time slot index q_i is transmitted by the EN, and the estimated time slot index $\hat{q}_i$ is misaligned due to the clock drift. To compensate for this frame misalignment, the estimated clock drift $\hat{T}_{\mathrm{d},j} + \hat{T}_{\mathrm{c},i}$ is subtracted from the reception timing.

C. Additional Overhead Required for Proposed Method

As discussed in this section, we consider the additional overhead required for performing the proposed clock drift estimation and compensation method. Because clock drift can be estimated and compensated during time slot detection, as shown in (16) and (19), the additional computational complexity is significantly low. Meanwhile, the GW needs to store float

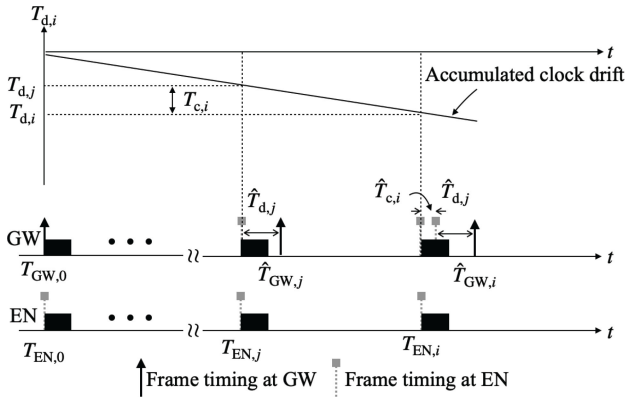


Fig. 7. Example of clock drift compensation with $\mu < 0$ and $\sigma^2 = 0$. As an example, we set $q_j = q_i = 0$.

type data (time related variables, i.e., $t_{GW,0}$, $t_{GW,j}$, $t_{GW,i}$, T_{slot}, T_{frame}, T_{offset}, $\hat{T}_{GW,i}$, $\hat{T}_{d,j}$, and $\hat{T}_{c,i}$) and int type data (nontime related variables, i.e., i, j, and q_{max}) to solve (16) and (19) if neither the time slot length nor the frame length is common among the ENs. It should be noted that the sizes of the float and int data types are 4 and 2 bytes, respectively. Hence, the additional memory usage at the GW can be determined as $M = 9 \times 4 + 3 \times 2 = 42$ [byte]. Thus, the total additional memory usage is MN [byte], where N denotes the number of ENs.

V. Implementation of PLIM With Clock Drift Estimation and Compensation Scheme

In this study, we developed a PLIM using the proposed clock drift estimation and compensation scheme and evaluated its practicability. The packet generation interval is set to $T_{frame} = \{30, 130\}$ [s], and the time slot length is set to $T_{slot} = 1000$ [ms] , irrespective of the value of T_{frame}.[2] The transmission timing offset is set to $T_{offset} = \{0, 300, 500\}$ [ms], and the number of frequency channels is $K = 2$. Owing to the limited capability of LoRaWAN GW (Dragino LG-01), two LG-01s with carrier frequencies of $f_c = 924.0$ [MHz] and 924.2 [MHz] are used as a virtual GW with $K = 2$. For the initial synchronization and calculation of the initial clock drift, $\hat{T}_{d,1}$ in (20), an EN transmits the first and second packets as a confirmed message to receive the ACK signal from the GW. If the EN cannot receive the ACK signal for the two continuous confirmed messages, it restarts the initialization.

A. PLIM Operation

Fig. 8 illustrates the spectrogram measured using the spectrum analyzer (Tektronix RSA306-B). The figure depicts the proposed PLIM operation, and the EN determines the combination of the time slot and frequency channel (index) based on the transmit data sequence. We set $K = 1$ to evaluate the proposed clock drift estimation and compensation scheme, which does not affect the frequency channel index detection.

[2]The optimization of T_{slot} for different values of T_{frame} is outside the scope of this study.

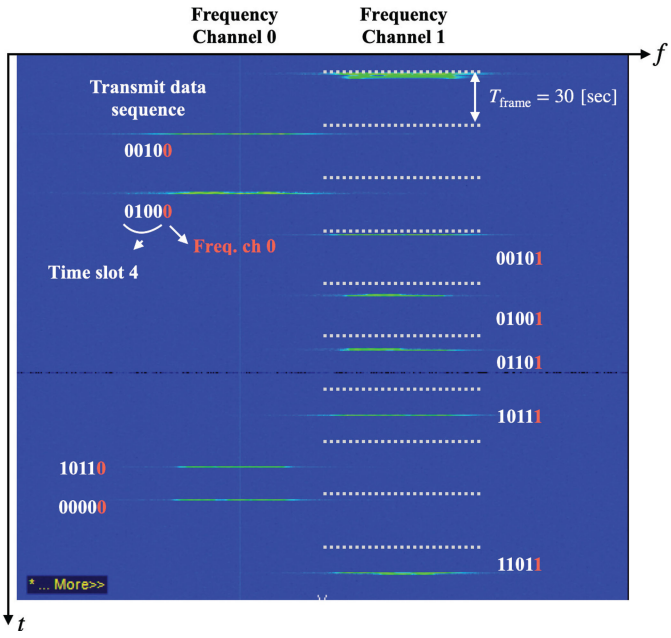


Fig. 8. Spectrogram of LoRaWAN with PLIM.

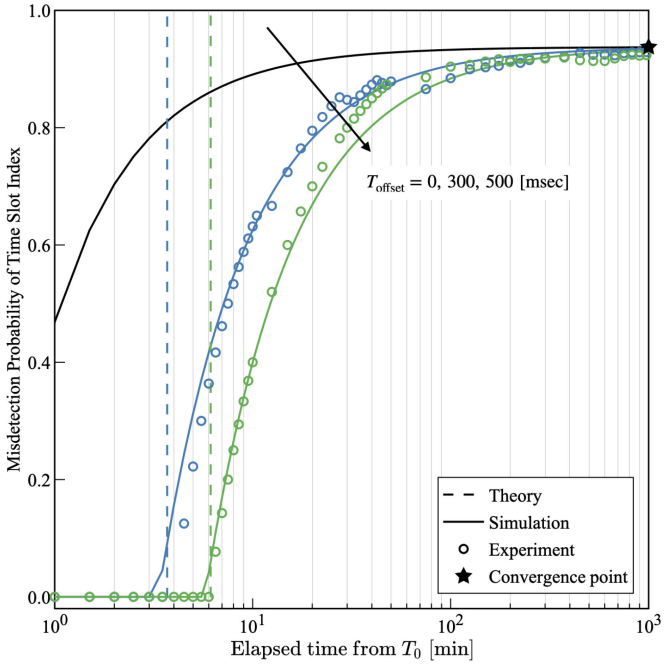
The following sections present the experimental and simulation results (averaged over 100 000 simulation runs) to validate the effectiveness of the proposed clock drift estimation and compensation scheme.

B. Impact of Transmission Timing Offset

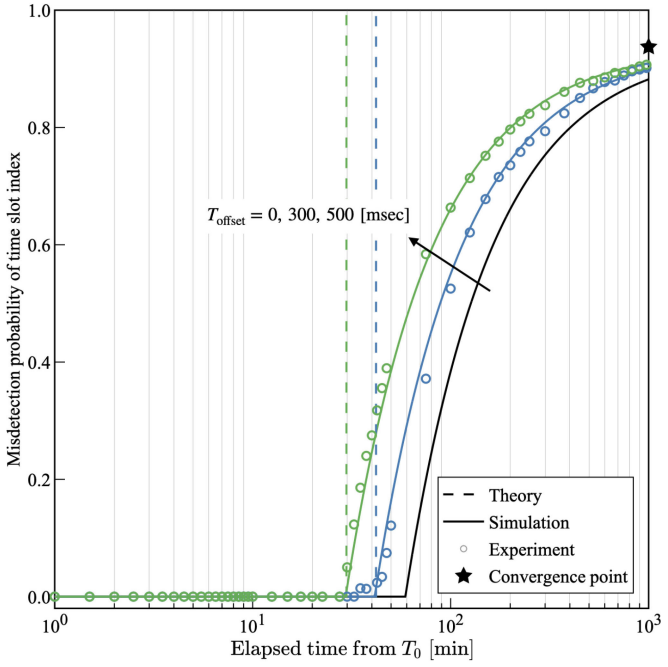
In (17), the transmission timing offset T_{offset} plays an important role in absorbing the small clock drift. Fig. 9 depicts the impact of the transmission timing offset T_{offset} on the time slot index misdetection probability, when no clock drift estimation and compensation is performed. The packet generation interval is set to $T_{frame} = 30$ [s]. EN 1 and EN 2 are selected as representatives of the EN because they exhibit positive and negative clock drifts. For the simulation, the clock drift is added as $\mathcal{N}(\mu, \sigma^2)$, where μ and σ^2 are obtained from Table II. In the figure, the solid lines represent the simulated results, and the circles represent the experimental results. For confirmation, the theoretically estimated timing at which the time slot index misdetection occurs is plotted, indicated by the dashed lines, and the convergence point of the misdetection probability without compensation is plotted in a star-shaped plot. The theoretical timing is calculated as follows. The clock of the node advances or delays μ [s] per unit time, on average, as presented in Table II. Thus, the first time slot misdetection occurs at data packet $i^\star$, wherein the following equation is satisfied:

$$i^\star = \begin{cases} \left\lceil \frac{T_{offset}}{|\mu| \times T_{frame}} \right\rceil & \text{for} \quad \mu < 0 \\ \left\lceil \frac{T_{frame} - T_{offset}}{|\mu| \times T_{frame}} \right\rceil & \text{for} \quad \mu \leq 0 \end{cases} \tag{21}$$

where $\lceil \cdot \rceil$ returns the smallest integer larger than or equal to the argument. Based on the values presented in Table II, the first time slot misdetection occurs at the $i^\star = (8, 13)$th data packets and $i^\star = (84, 60)$th data packets for EN 1 and EN 2 with $T_{offset} = (300, 500)$ [ms], respectively. The convergence

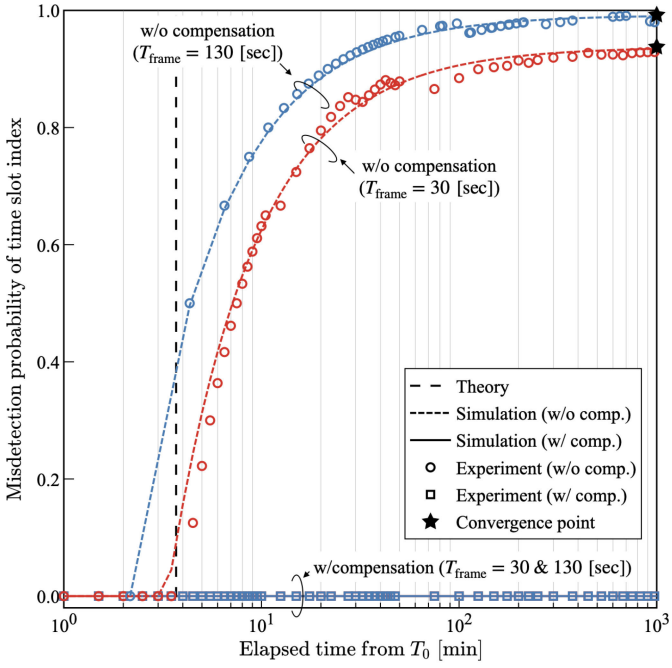


(a)

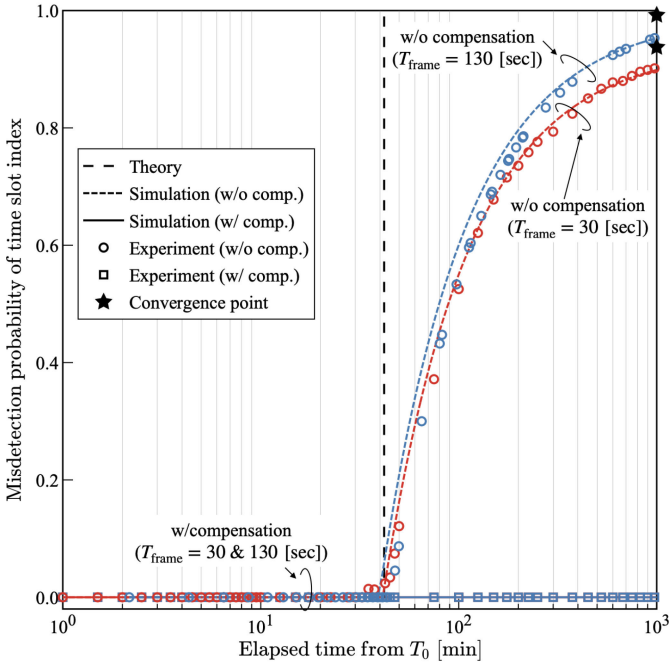


(b)

Fig. 9. Impact of transmission timing offset T_{offset} on misdetection probability of time slot index, with packet generation interval $T_{\text{frame}} = 30$ [s]. (a) EN 1. (b) EN 2.



(a)



(b)

Fig. 10. Effectiveness of proposed clock drift estimation and compensation scheme, with transmission timing offset $T_{\text{offset}} = 300$ [ms]. (a) EN 1. (b) EN 2.

point of the misdetection probability is calculated as follows. Without compensation, the probability of accurate detection of the time slot index is asymptotically equal to $(1/q_{\max})$, where $q_{\max}$ denotes the number of time slots expressed as (1). This is because of the random information bit generation following the misdetection. Thus, the misdetection probability converges to $1 - (1/q_{\max})$ over time. Considering $T_{\text{frame}} = 30$ [s], a convergence point of 93.8% occurs. It often takes approximately 200 [ms] to start data packet transmission from the data sequence generation at the EN owing to the limited capability. Thus, only the experimental results with $T_{\text{offset}} = 300$ and 500 [ms] are presented.

The experimental results agree well with the simulated and theoretically estimated results. As time elapses from T_0, the misdetection probability increases owing to the accumulated clock drift. When the accumulated clock drift exceeds the time slot boundary, the GW detects an incorrect time slot index. For EN 1, setting a sufficiently large T_{offset} makes the time slot

detection more robust against the clock drift. Meanwhile, the misdetection probability of EN 2 worsens as T_{offset} is set to larger values. This can be explained by Fig. 4 and Table II, which indicate that the mean values of the normalized clock drift are negative for EN 1 ($\mu_1 = -1.36$ [ms]) and positive for EN 2 ($\mu_2 = 0.28$ [ms]). Thus, considering the receiving GW, the clock speed is faster at EN 1 and slower at EN 2. Thus, setting a large T_{offset} value is suitable for EN 1 but not for EN 2.

The experimental curves exhibit a zigzag shape for the following reasons. Because the time slot index is $q_i \in \{0, \ldots, q_{\max} - 1\}$, if the estimated time slot index $\hat{q}_i$ is outside this range, it can be compensated to either 0 or $q_{\max} - 1$, as shown in (17). Thus, the misdetection probability decreases slightly; however, owing to the accumulated clock drift, misdetection occurs again. Misdetection may also be avoided by performing recalibration immediately before packet $i^\star$, which requires only the calculation of the initial clock drift $\hat{T}_{\text{d},1}$ in (20) and the estimated first misdetection packet index $i^\star$ in (21). However, this approach has two main drawbacks. First, the GW needs to inform each EN of when to reperform the synchronization process, which requires the downlink packet transmissions from the GW to each EN. During the synchronization process, the EN cannot transmit additional information bits through the information-bearing index because two consecutive data packets must be transmitted in predetermined time slots, thereby wasting radio resources. Second, the clock drift may vary due to several factors, including temperature change and packet delay. Thus, the actual misdetection may occur at some packet i earlier than the predicted packet index $i^\star$.

C. Effectiveness of Proposed Clock Drift Estimation and Compensation Scheme

Fig. 10 depicts the experimental results of the misdetection probability of the time slot index. The packet generation interval is set to $T_{\text{frame}} = \{30, 130\}$ [s], i.e., the convergence point of the misdetection probability is $\{93.8, 99.2\}$ [%], and the transmission timing offset is set to $T_{\text{offset}} = 300$ [ms]. Fig. 10 depicts that the experimental and simulation results agree well with each other. The averaging effect of the simulation results leads to a difference between the experimental and simulation results. The misdetection probability increases as time elapses when the clock drift is not compensated. In contrast, the misdetection probability is maintained at 0 when the proposed clock drift estimation and compensation scheme is applied.

D. Performance of Proposed Scheme Under Large Number of ENs

Both the experimental and computer simulation results confirm that the proposed clock drift estimation and compensation scheme provides satisfactory results. However, owing to the limitation of the experimental setup, it is difficult to evaluate its performance under a large number of ENs, which can cause frequent packet collision. Such packet collisions may have a significant impact on the proposed scheme because some ENs cannot update the clock drift based on (19) at each

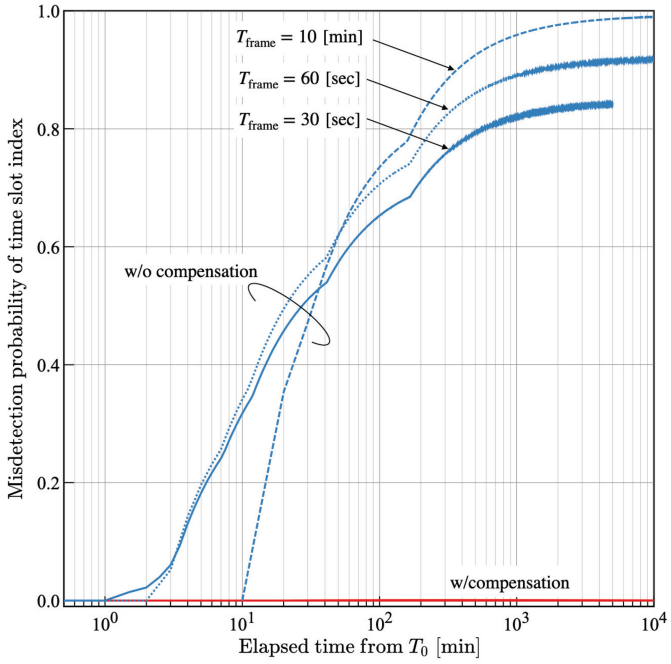


Fig. 11. Impact on multiple ENs.

packet transmission. To evaluate the impact of packet collision on the proposed scheme, computer simulations with a large number of ENs are performed. In this simulation, 100 ENs are considered, and the packet generation interval is set to T_{frame} as a parameter. The number of available frequency channels is set to $K = 16$. Each EN has its inherent clock drift, whose mean value and variance are randomly selected from the values listed in Table II. Table I lists the other simulation parameters. Fig. 11 depicts the misdetection probability of the time slot index as a function of the elapsed time from T_0. The misdetection probability immediately increases if no countermeasure is taken for the clock drift. For example, even the third packet cannot be accurately received when $T_{\text{frame}} = 10$ [min]. Conversely, the figure clearly shows that the proposed clock drift estimation and compensation scheme can detect the time slot index accurately, even for large values of T_{frame} when a large number of ENs exist and packet collision happens with a high probability.

VI. Conclusion

In the PLIM, a GW retrieves a transmit bit sequence from the time at which each EN transmits a data packet. Ideally, stringent synchronization between each EN and GW is required. However, synchronization is lost because of the inexpensive RTC oscillator on each EN. Once synchronization is lost, misdetection of the time slot index occurs, which deteriorates the performance improvement caused by PLIM. This study proposes a clock drift estimation and compensation scheme for PLIM that does not incur any additional computational burden on the EN side as the entire operation is performed at the GW side. First, experimental measurements are conducted using the commercially available LoRaWAN GW and ENs to model the relative clock drift between a GW and each EN as a Gaussian random variable with small variances. A time slot index detection with a simple clock

drift estimation and compensation scheme is proposed based on this observation. Subsequently, a PLIM with the clock drift estimation and compensation method is implemented in a commercially available LoRaWAN EN and GW. The computer simulation results and experimental results indicate that the proposed clock drift estimation and compensation scheme enables the GW to accurately detect the time slot index even in the presence of clock drift. Experimental evaluations have shown that the PLIM with this proposed clock drift estimation and compensation scheme can be implemented without modifying any standardization of LoRaWAN.

This article focused on applying the proposed clock drift compensation method to LoRaWAN with PLIM. The proposed clock drift estimation and compensation method can be applied to the LoRaWAN system with periodic traffic. By compensating the clock drift at the GW, stringent synchronization between EN and GW is no longer necessary. Since the GW can virtually synchronize with each EN, the GW can adjust the downlink transmission timing. This allows the EN to shorten the receive window and save energy. The application of the proposed clock drift estimation and compensation method to the general LPWAN system is left as a future study.

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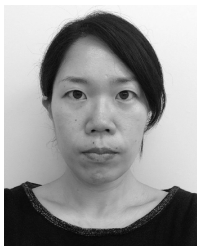

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